Electronic Information Disclosure Statement

DIFFUSED EXTRINSIC BASE AND METHOD FOR FABRICATION

Application:

Confirmation:

Applicant(s): Marc Cantell

Docket Number: BUR920010036

Group Art Unit:

Examiner:

search string: (5761080 or 5629556 or 5593905 or 5439833 or 5268314 or 5117271 or 4860085 or 4495512 or 4252581 or 3904450).pn.

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Citation No.	Patent Number	Date	Bar Code	Patentee	Class	Subclass
	P01	5761080	1998-06-02		DeCamp, et al.	364	490
	P02	5629556	1997-05-13		Johnson	257	592
	P03	5593905	1997-01-14		Johnson, et al.	437	31
	P04	5439833	1995-08-08		Hebert, et al.	437	31
	P05	5268314	1993-12-07		Connor	437	31
	P06	5117271	1992-05-26		Comfort, et al.	357	34
	P07	4860085	1989-08-22		Feygenson	357	59
	P08	4495512	1985-01-22		Isaac, et al.	357	34

	P09	4252581	1981-02-24		Anantha, et al.	148	175
	P10	3904450	1975-09-09		Evans, et al.	148	175

Remarks

(Remarks are not for responding to an office action.)

IBM Technical Disclosure Bulletin, Vol. 26, No. 2, July 1983, "Transistor Collector Doping for Reduced Capacitance:, W.P. Dumke, p. 492. IBM Technical Disclosure Bulletin, Vol. 25, No. 4, September 1982, "Using a DoublyImplanted Polysilicon Layer for Forming Base and Emitter Regions:, C.G. Jambotkar, pp. 1987-1989. IBM Technical Disclosure Bulletin, Vol. 24, No. 7A, December 1981, "Polycide Bipolar Transistor Process", F. Barson, et al., pp. 3424-3426.

Signature

Examiner Name	Date